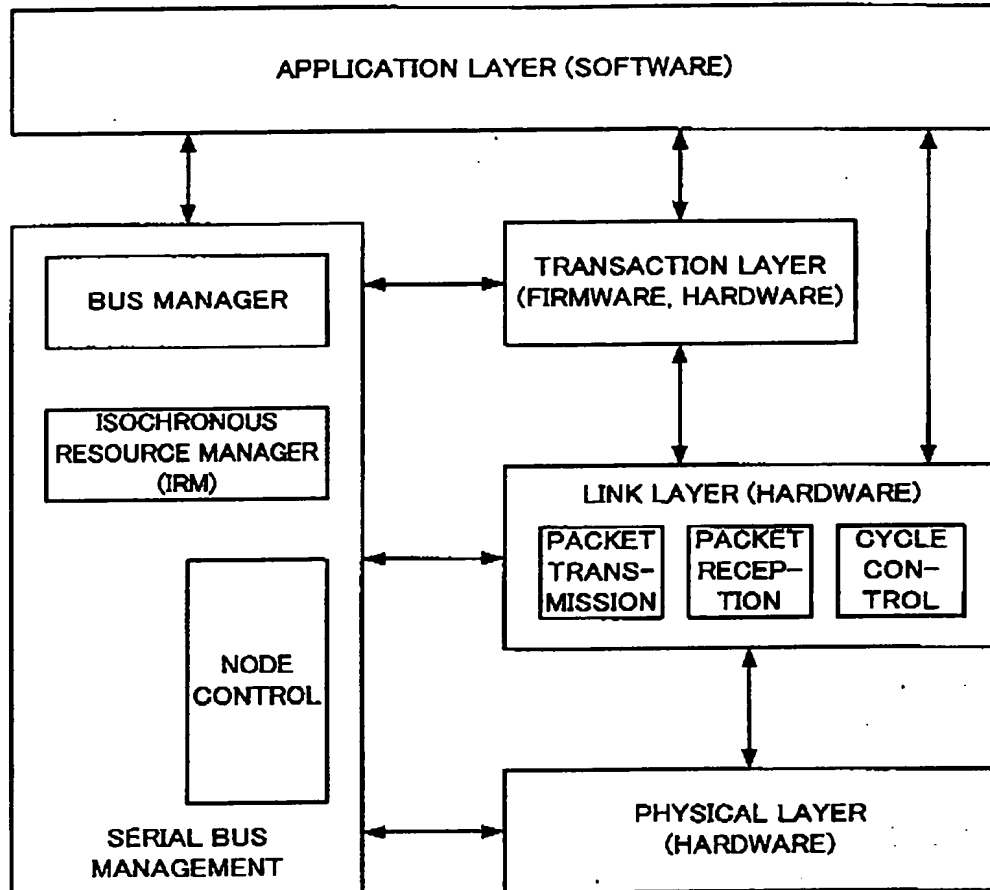


FIG.1



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FIG.2A

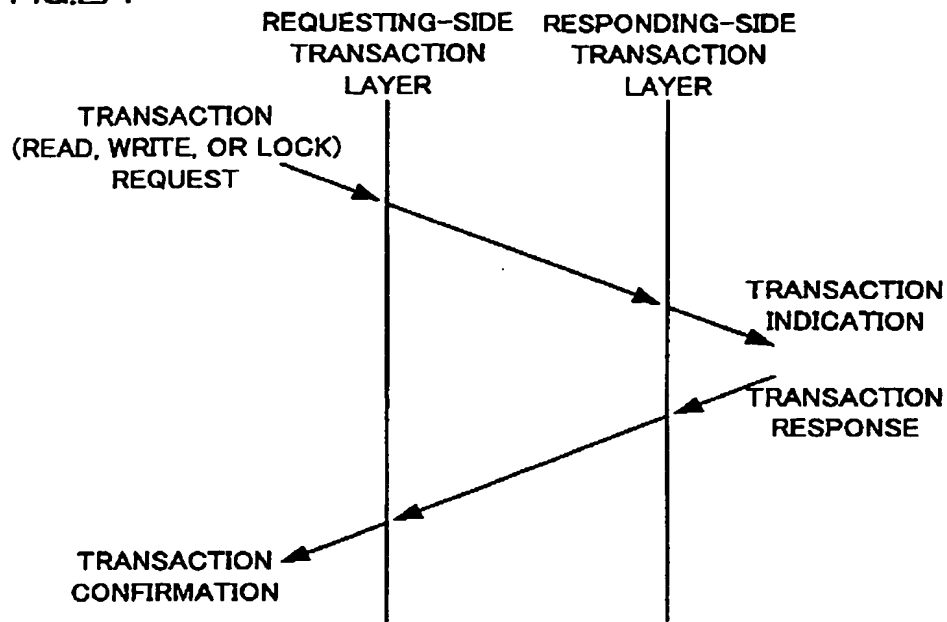
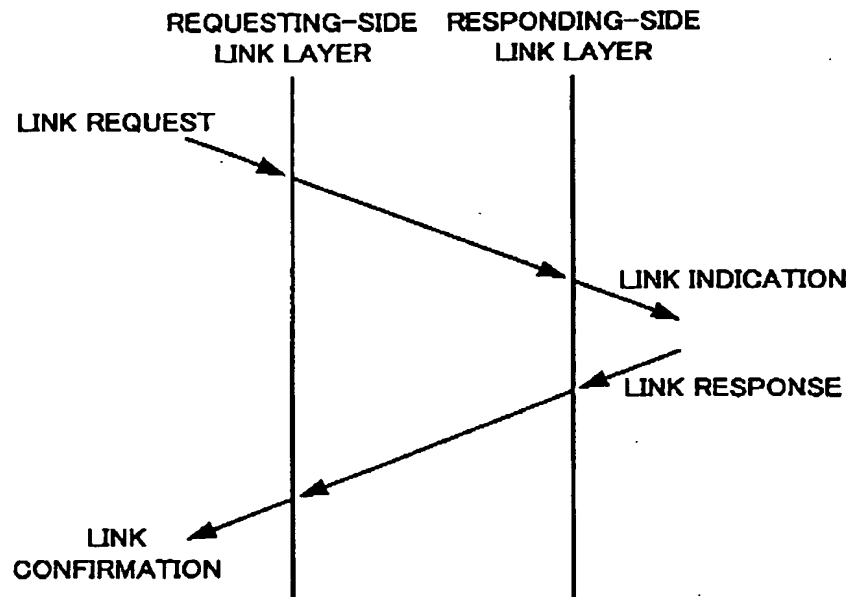
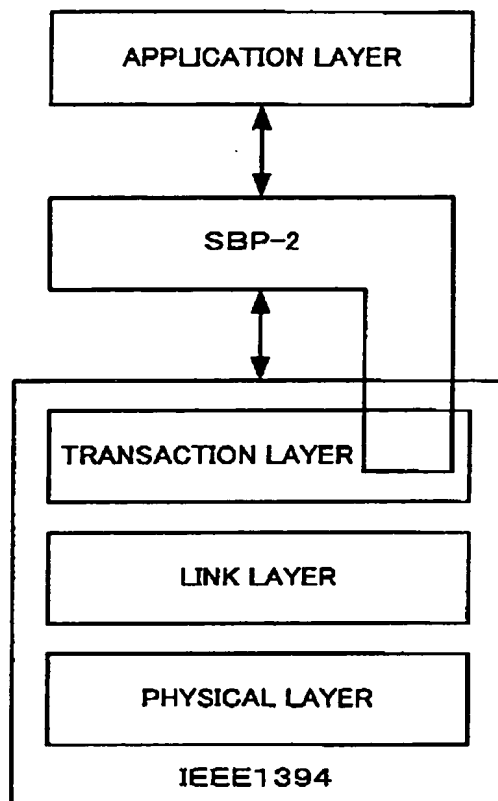


FIG.2B



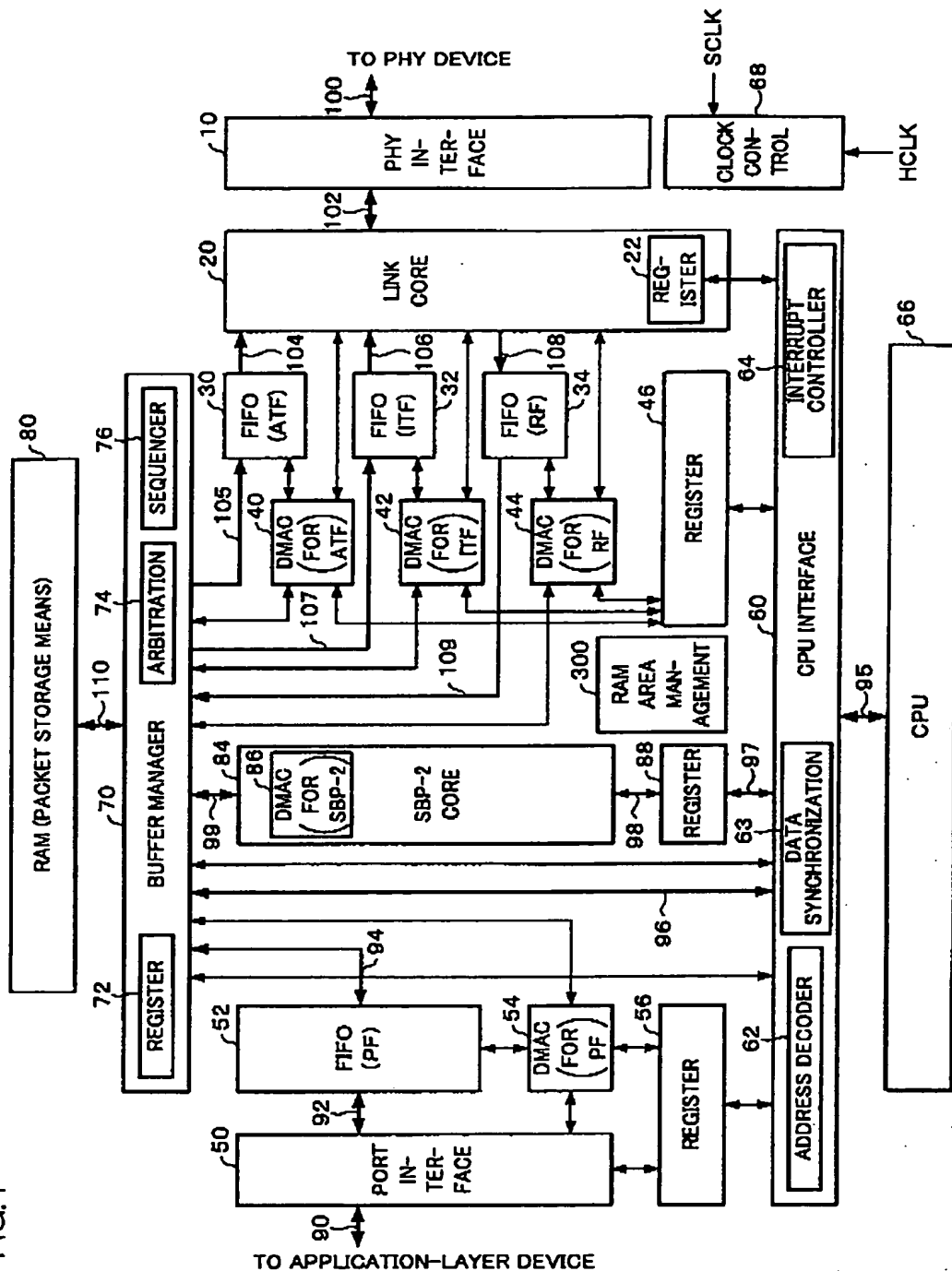
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FIG.3



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FIG. 4



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FIG.5

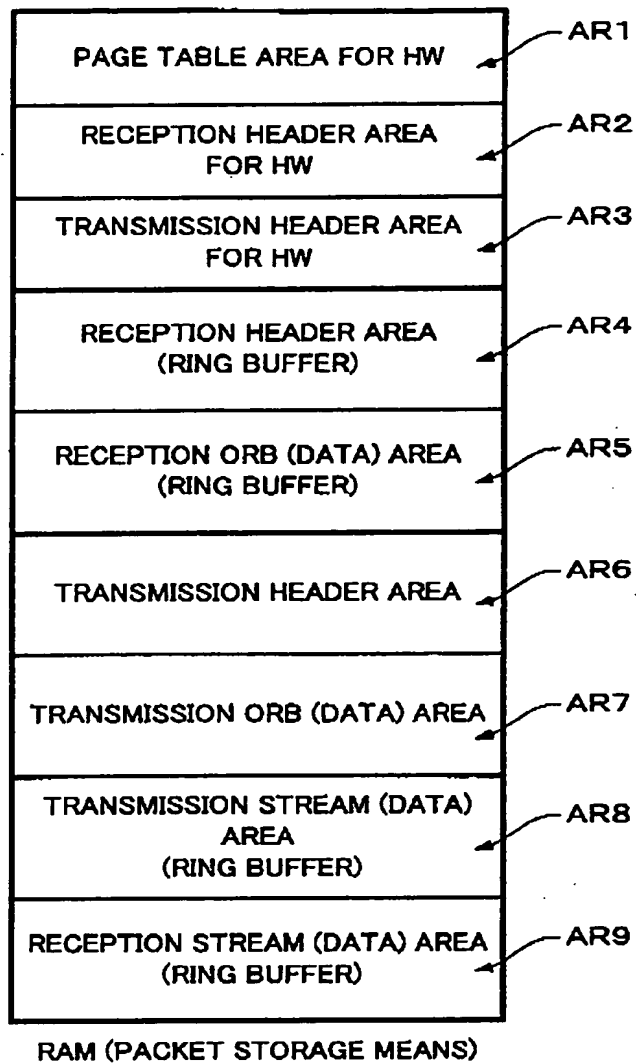
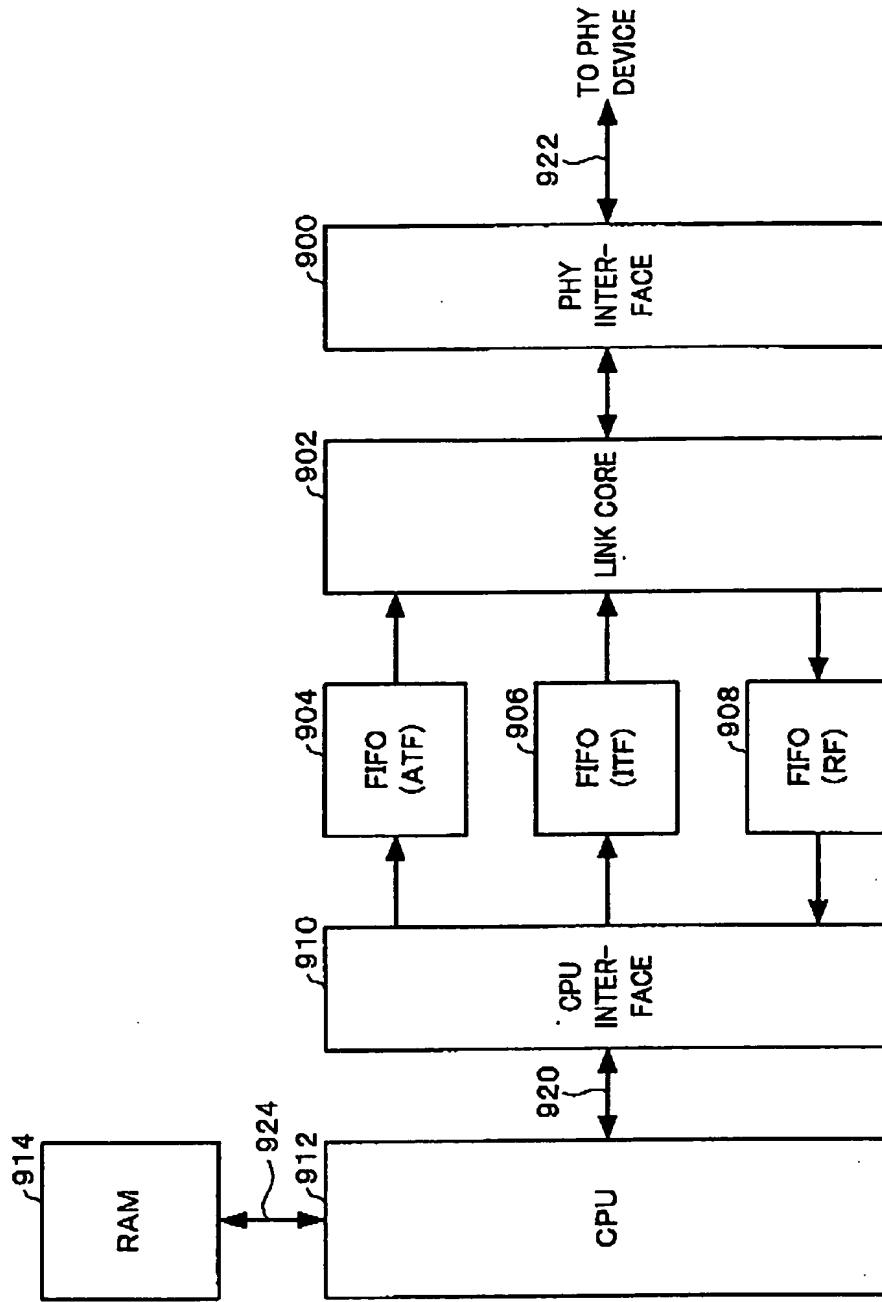
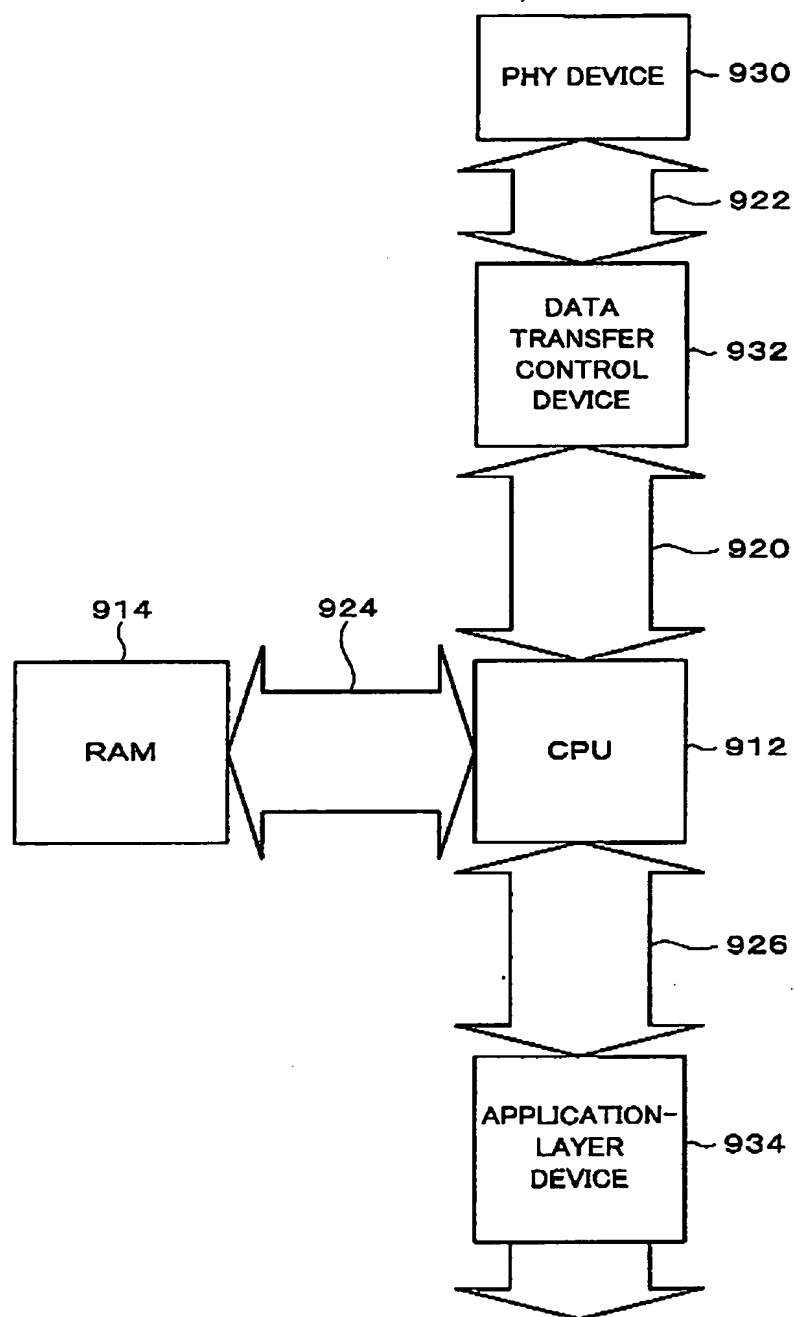


FIG. 6



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FIG. 7



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FIG.8

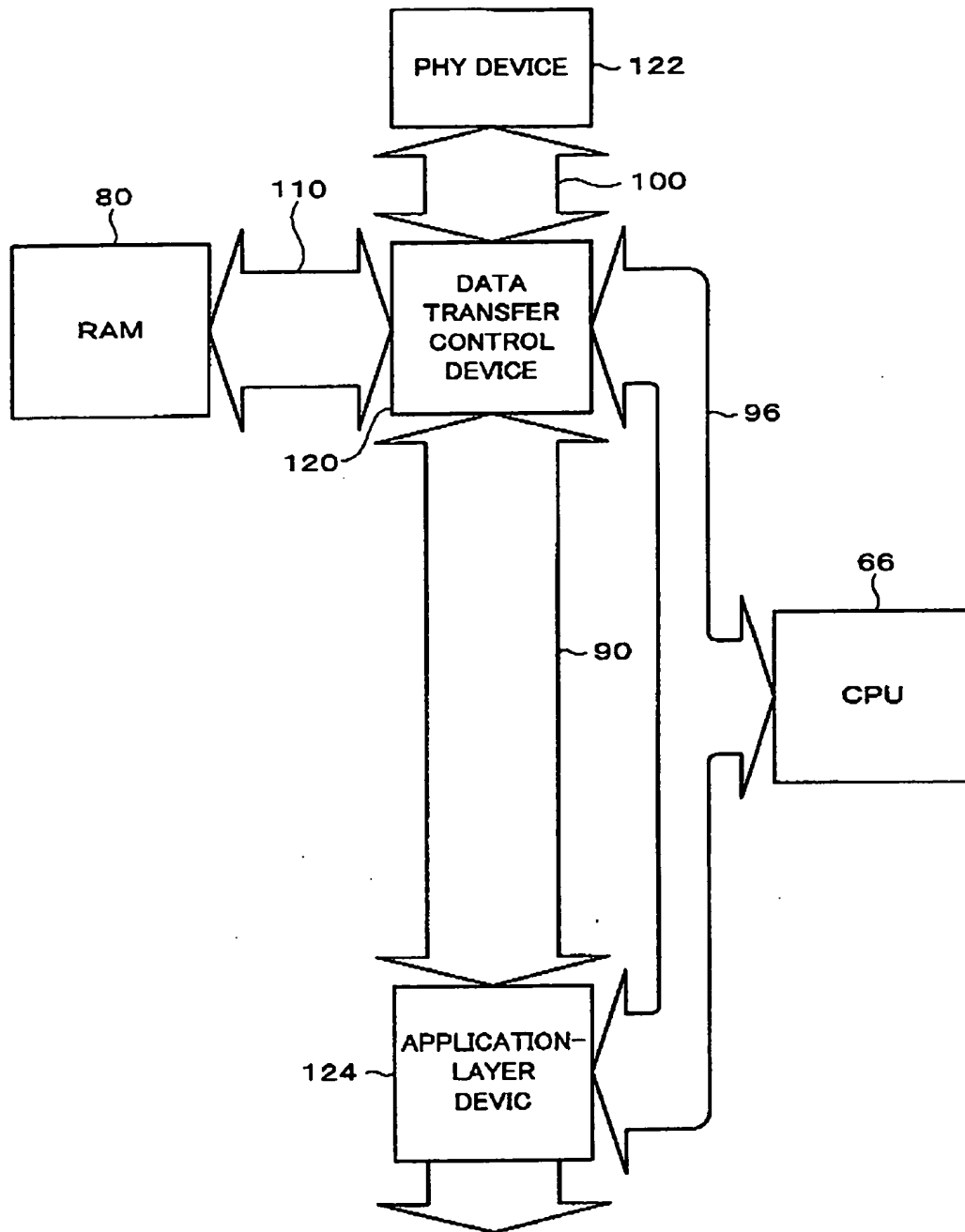


FIG. 8

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FIG.9A

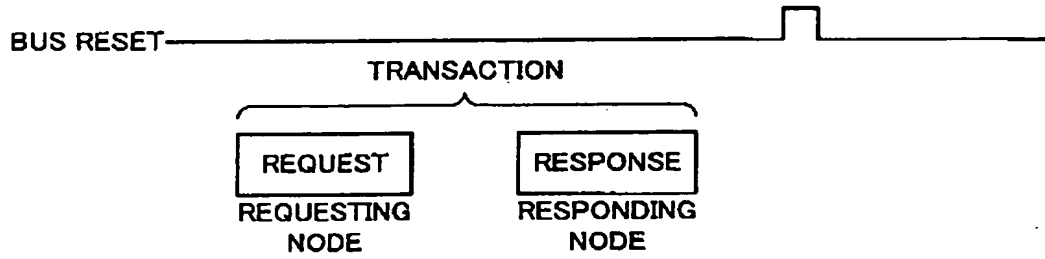
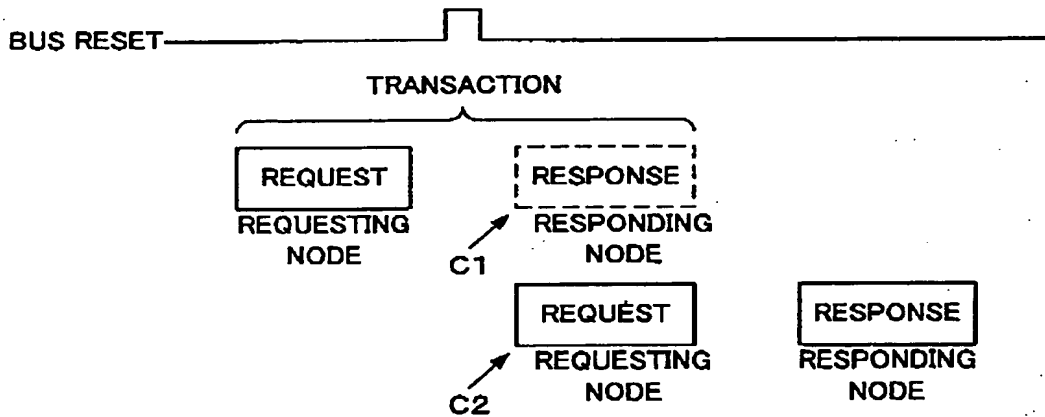
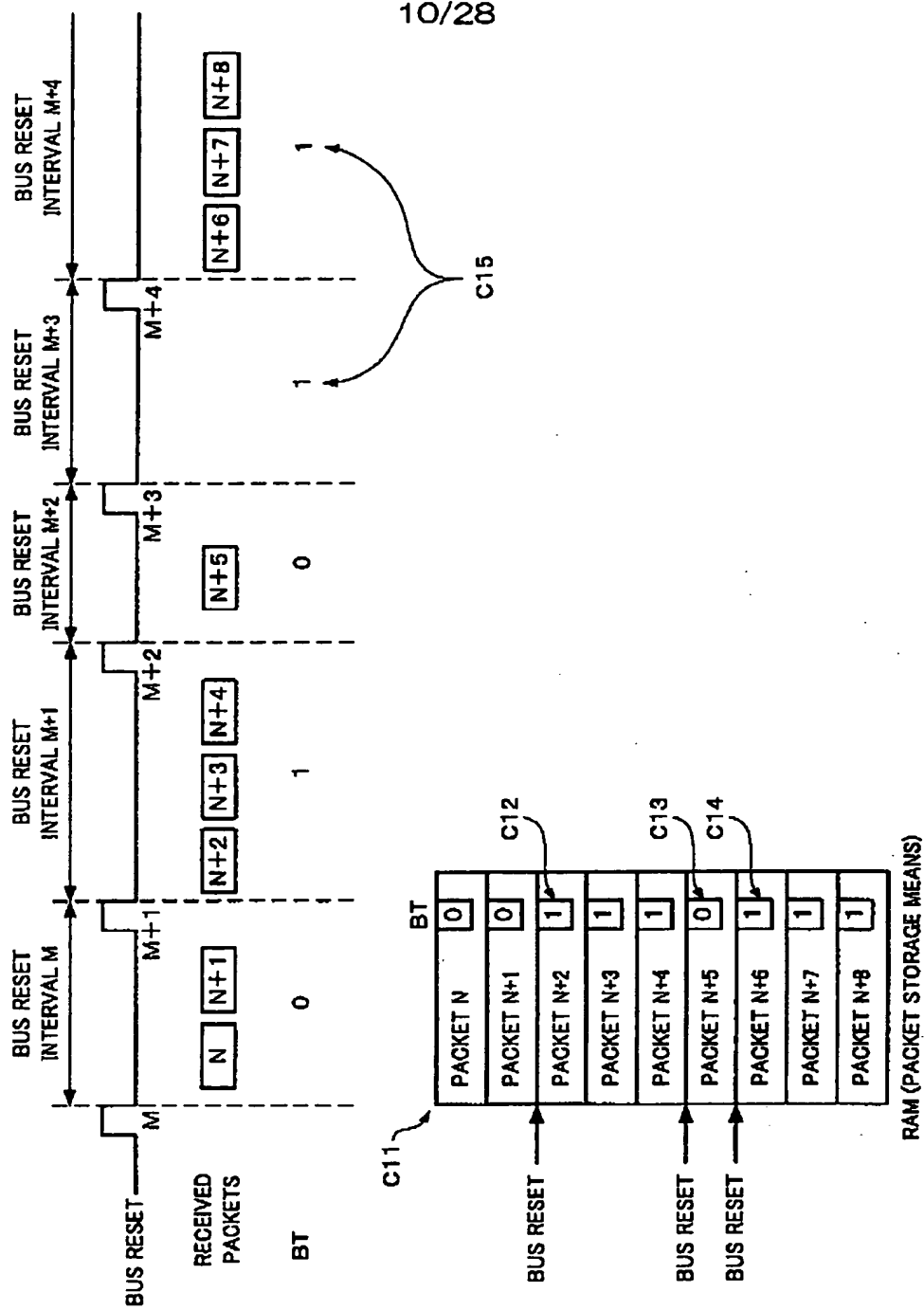


FIG.9B



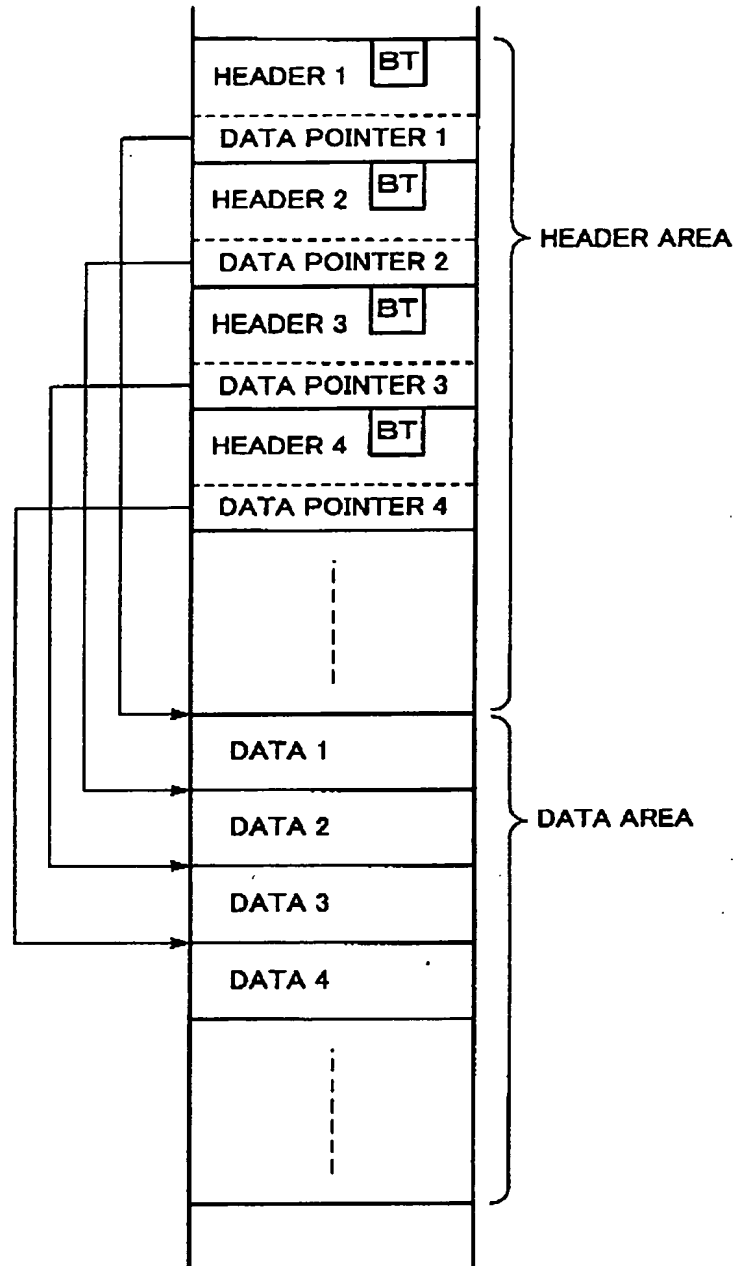
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FIG. 10



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FIG.11



RAM (PACKET STORAGE MEANS)

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FIG.12

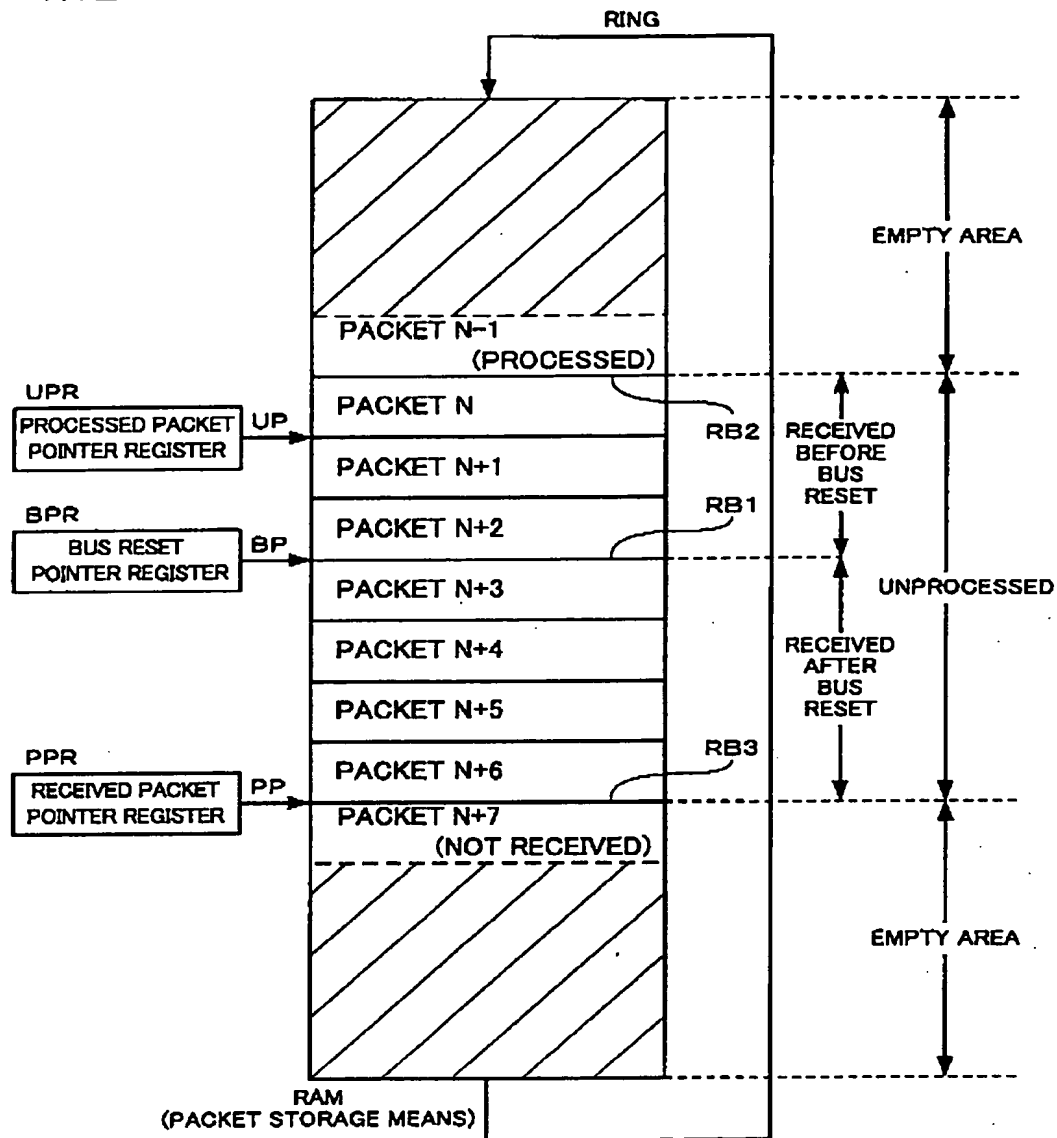


FIG.13A
COMPARATIVE EXAMPLE

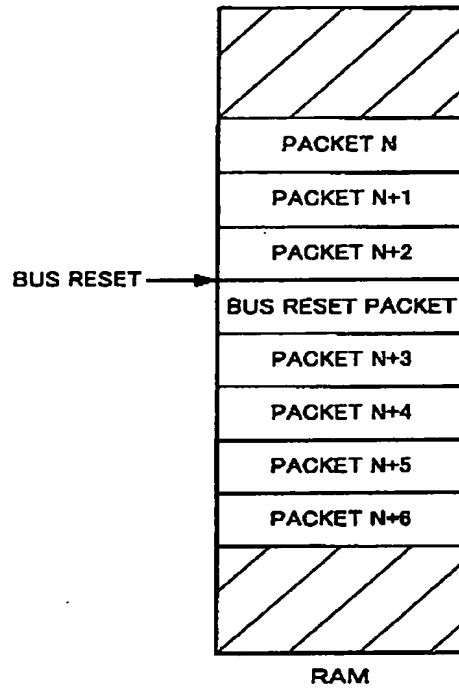


FIG.13B
METHOD USING BUS RESET PACKET

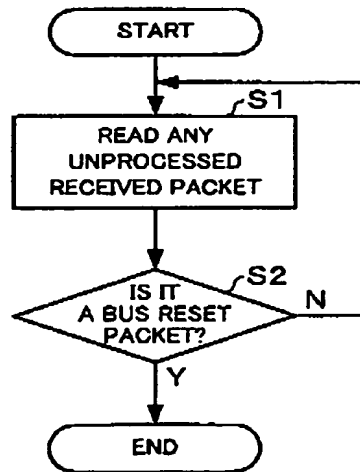
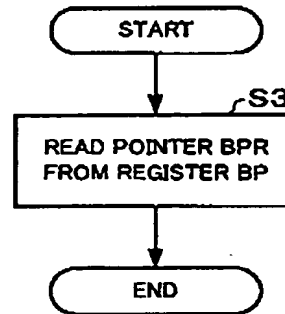
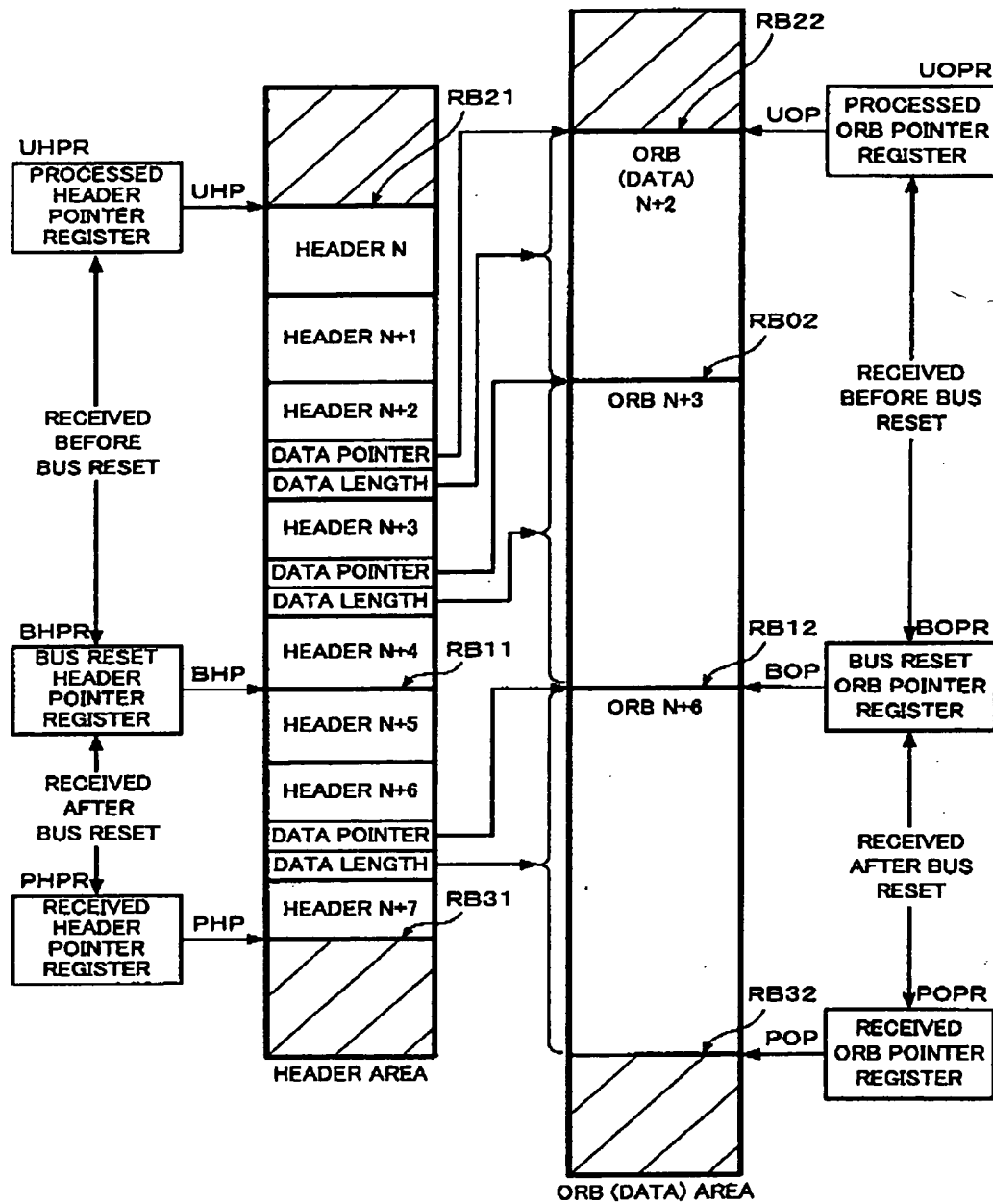


FIG.13C
METHOD USING BUS RESET POINTER



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FIG.14



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FIG.15A

METHOD USING BUS RESET HEADER POINTER ALONE

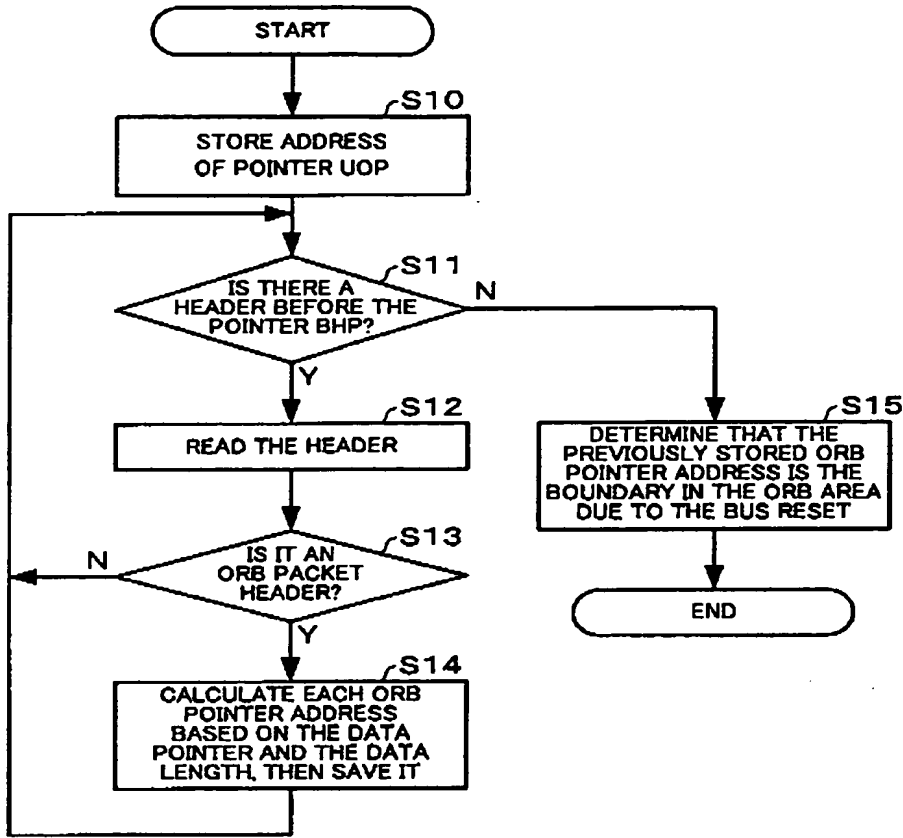


FIG.15B

METHOD USING BUS RESET ORB POINTER

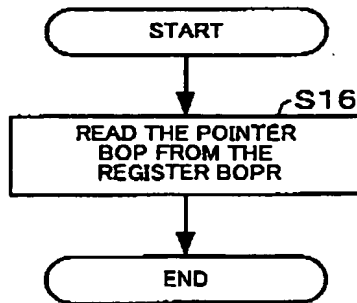
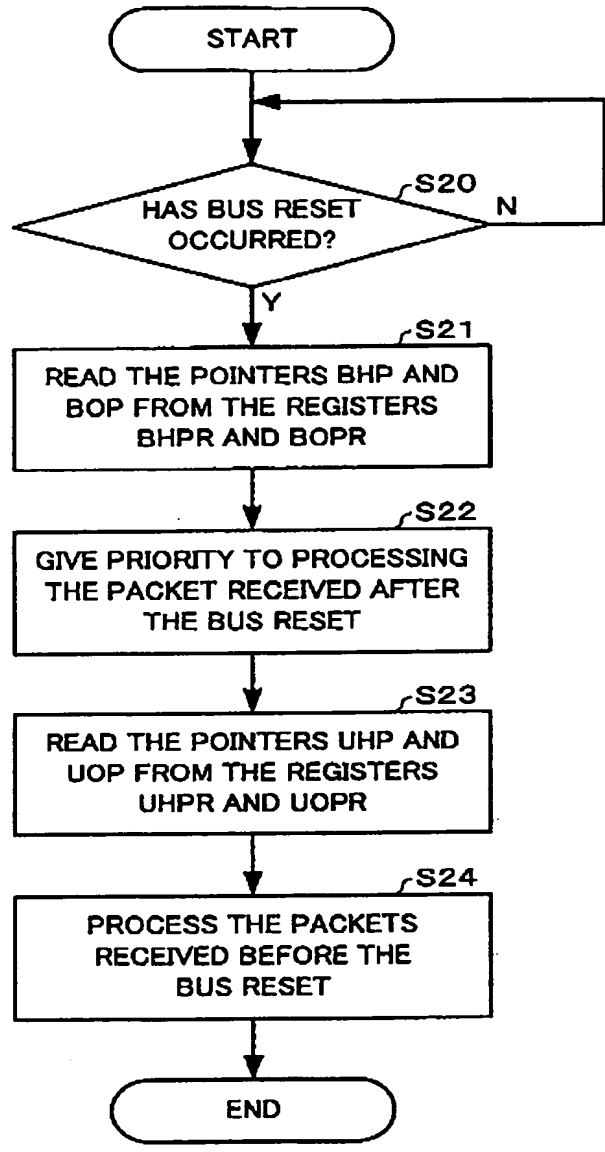


FIG.16



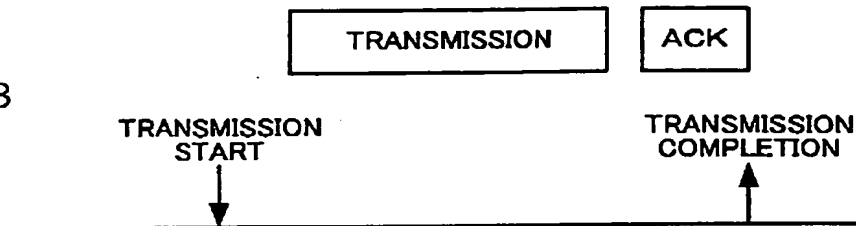
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FIG.17A



FIG.17B



BUS RESET

FIG.17C

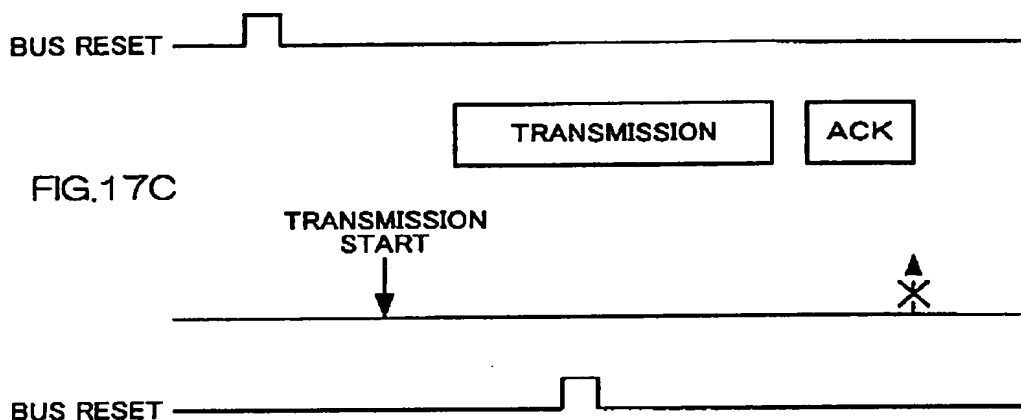
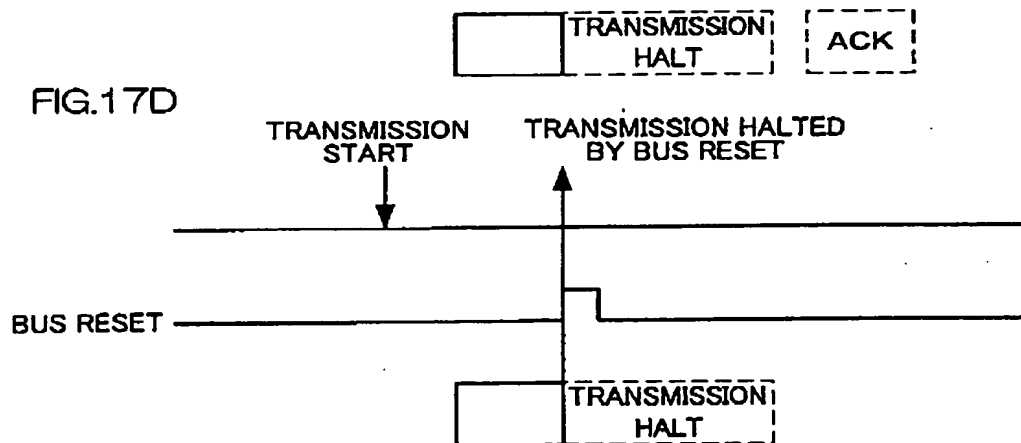


FIG.17D



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FIG.18A

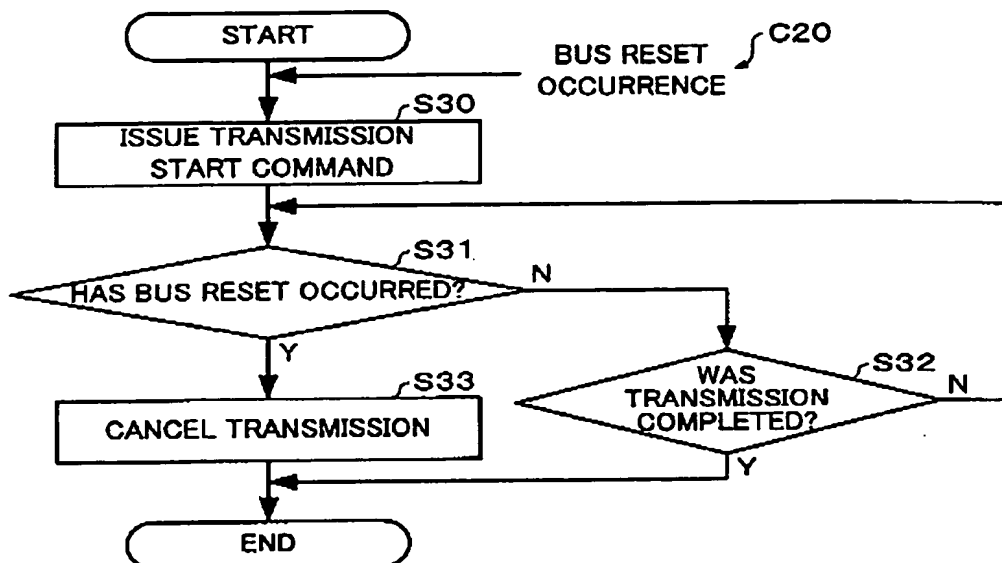


FIG.18B

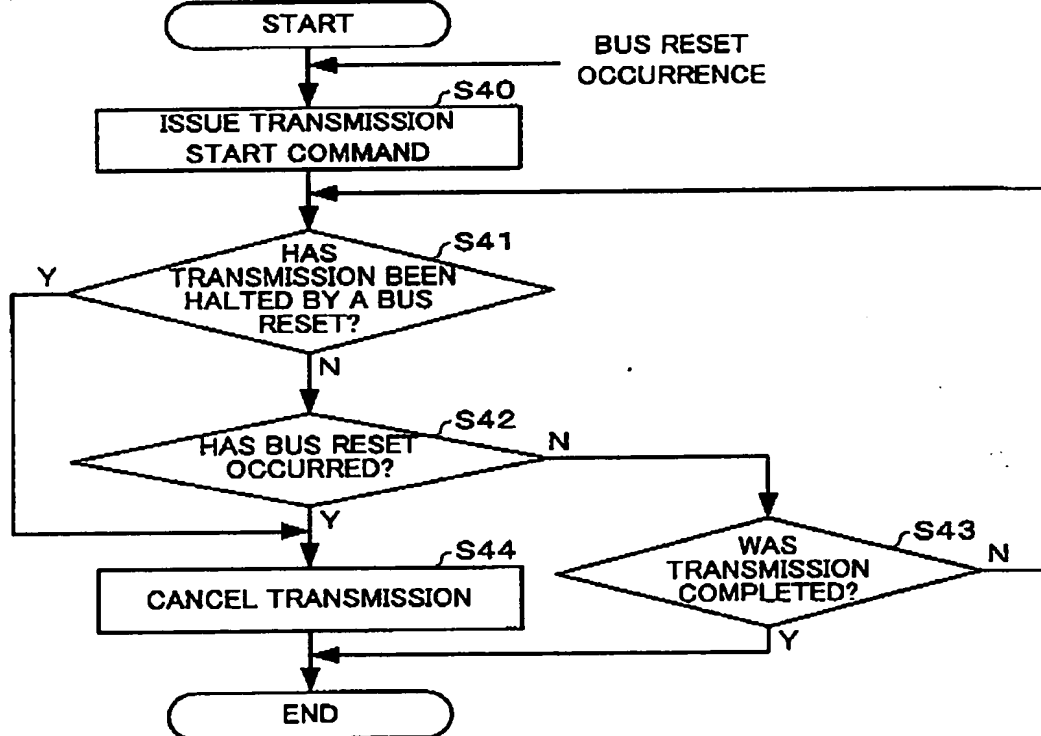


FIG. 19

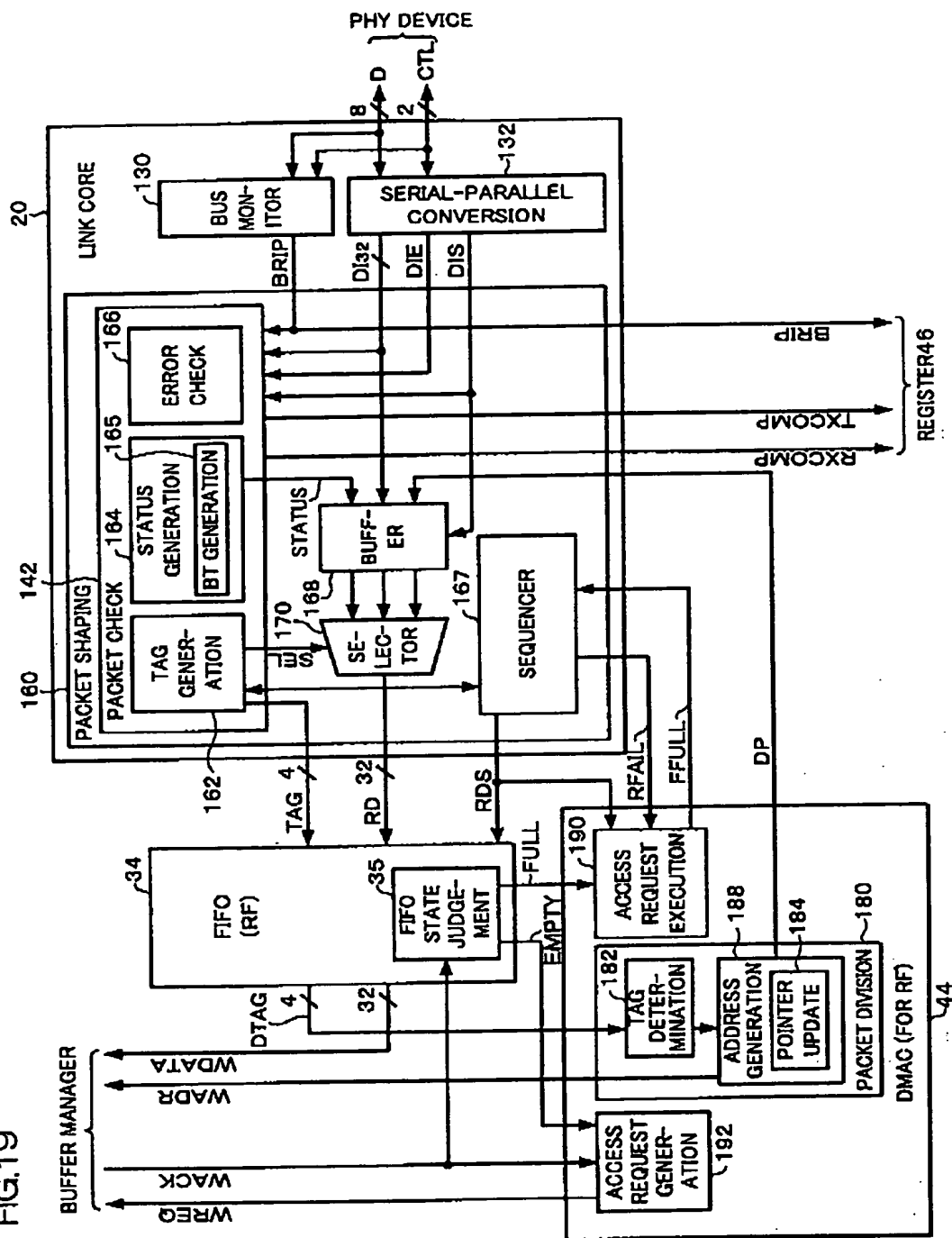


FIG.20A

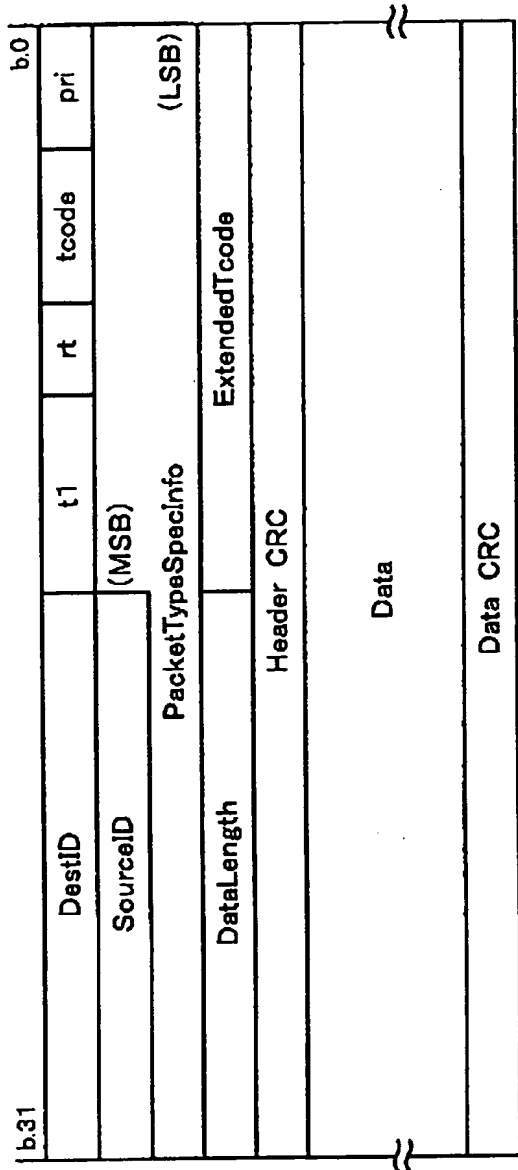


FIG.20B

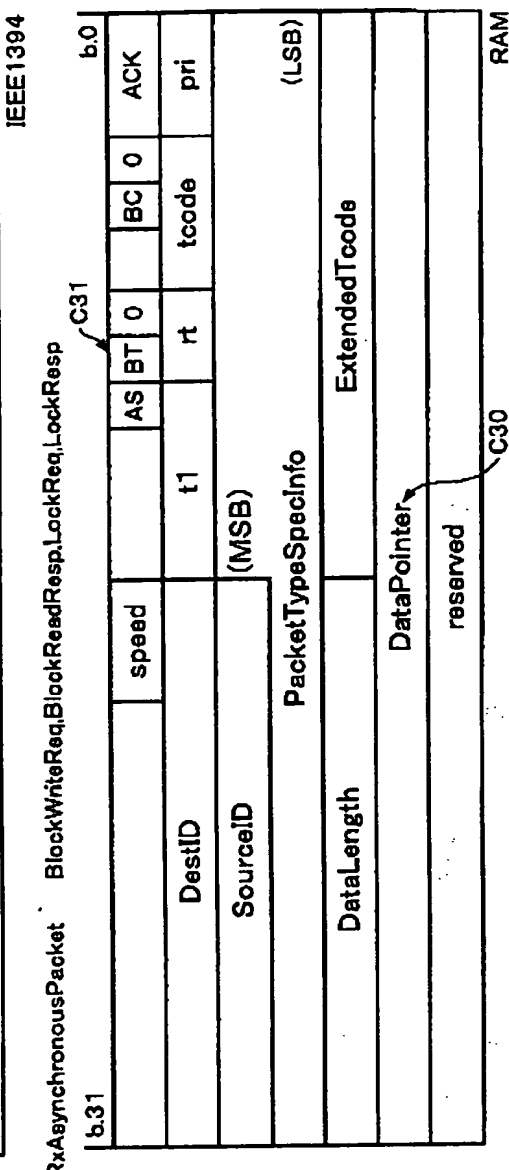


FIG.21

TAG(DTAG)	MEANING
0001	FW-SOP
0010	FW-HDR
0011	FW-FTR
0100	FW-ORB
0101	FW-STRM
1001	HW-SOP
1010	HW-HDR
1011	HW-FTR
1100	HW-ORB
1101	HW-STRM

FW FIRMWARE
HW HARDWARE
SOP START OF PACKET
(INITIAL QUADLET OF RECEIVED PACKET)
HDR HEADER OTHER THAN SOP
FTR ACK TRANSMISSION
ORB ORB (DATA)
STRM STREAM (DATA)

DEVICE RESET

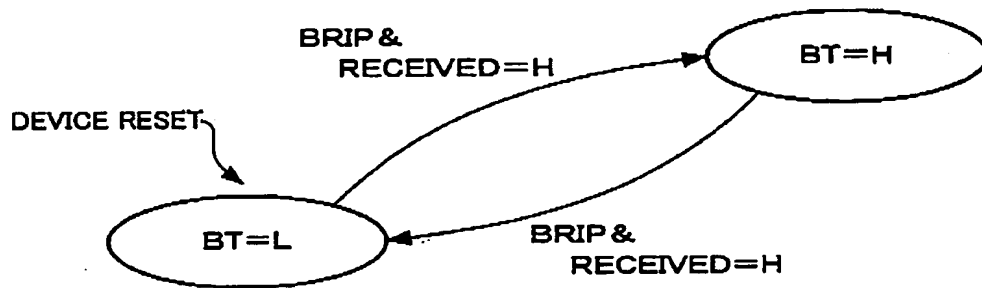
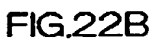
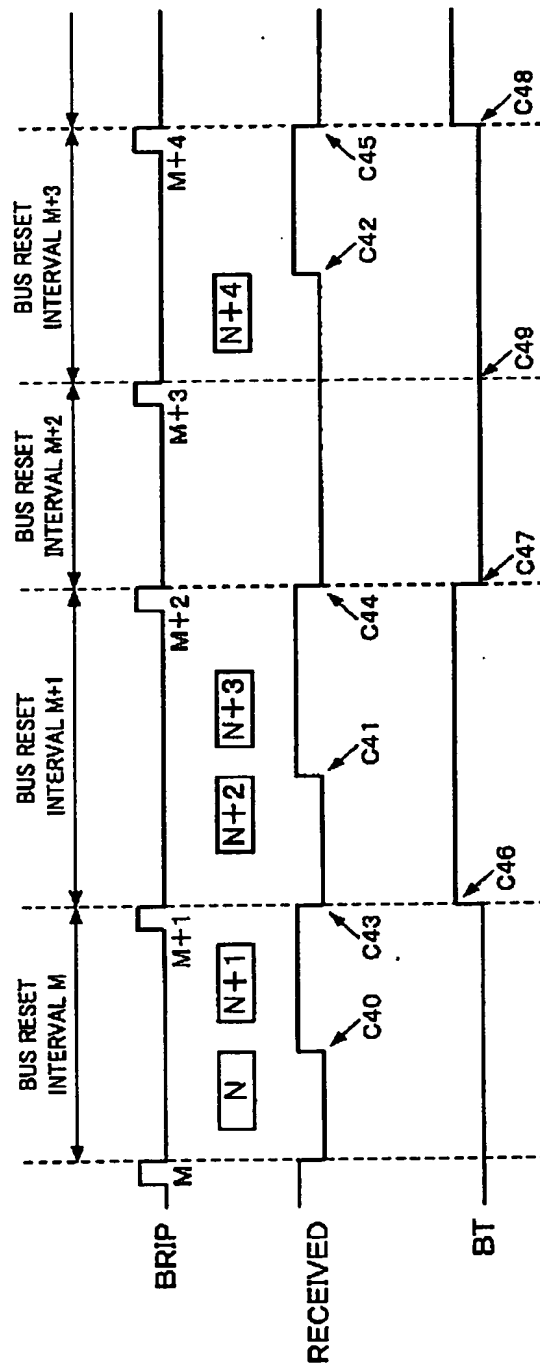


FIG.23



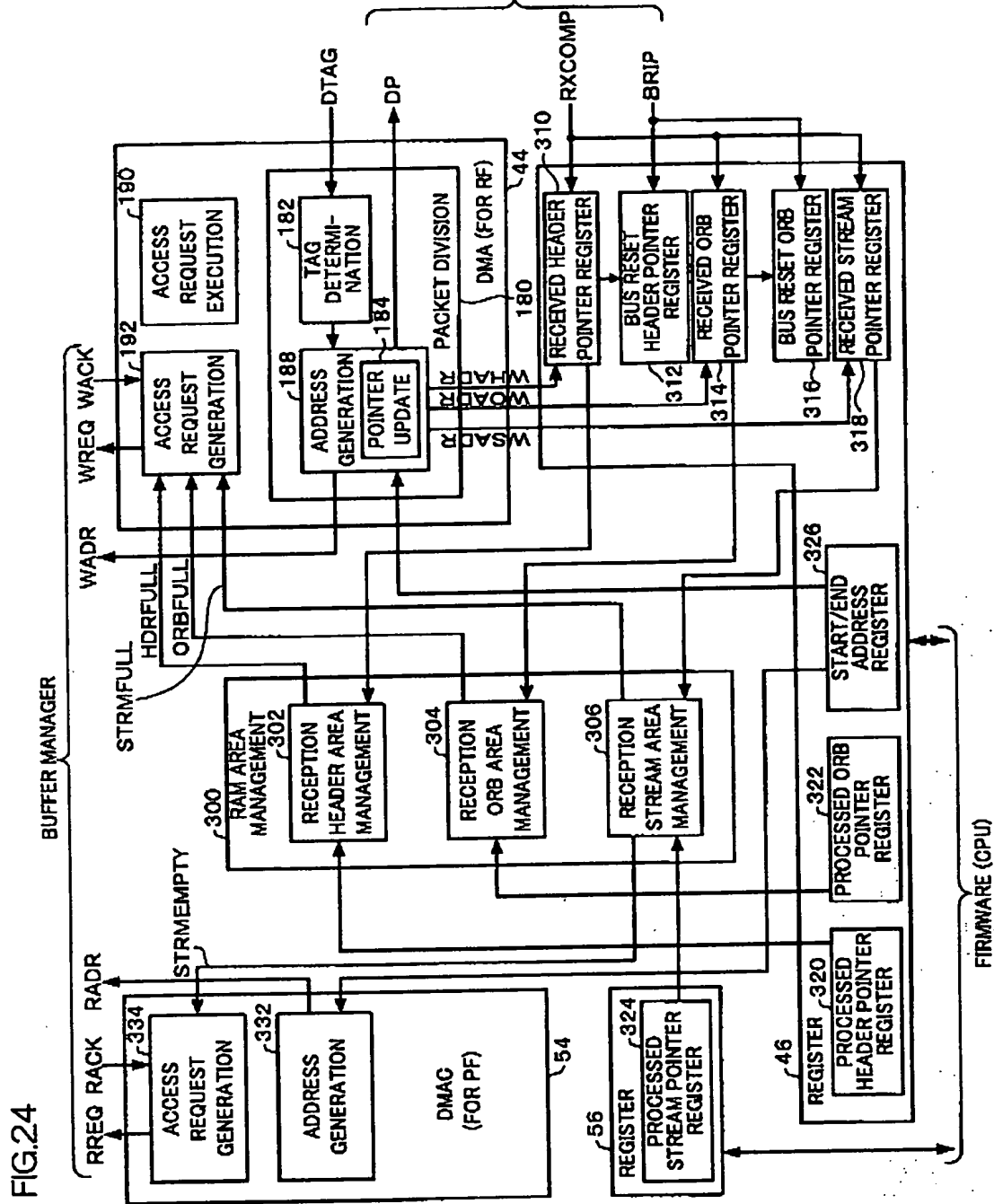


FIG.25

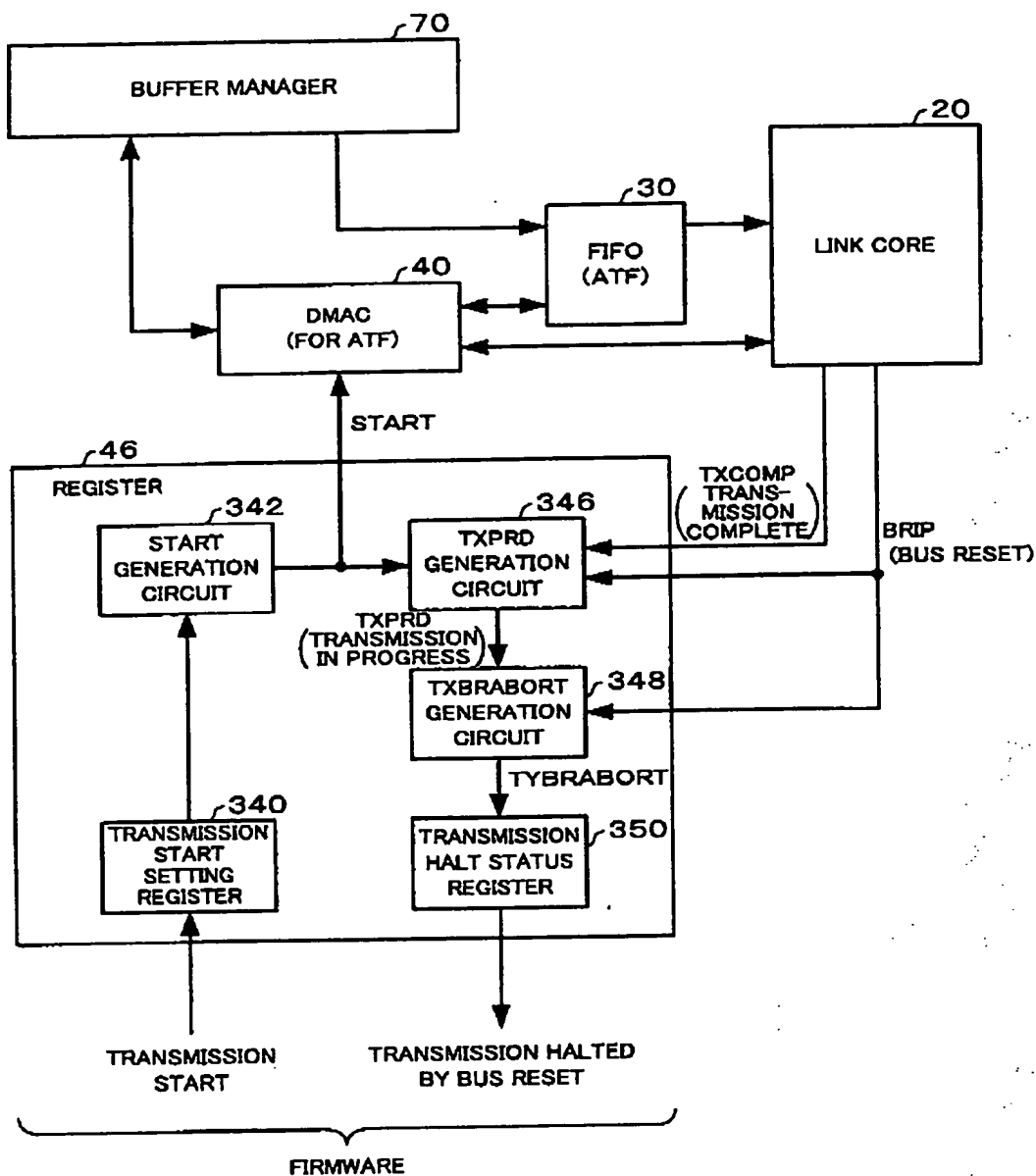
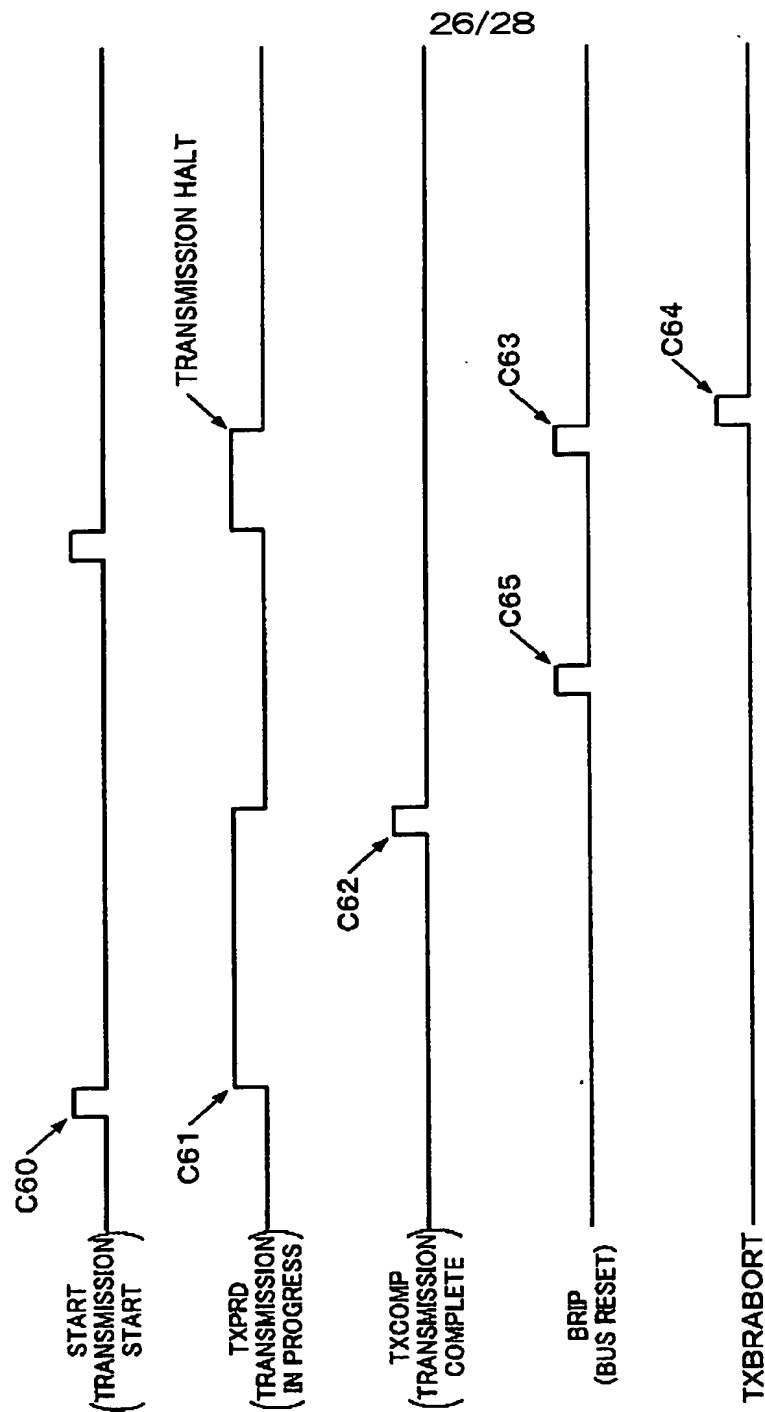


FIG.26



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FIG.27A

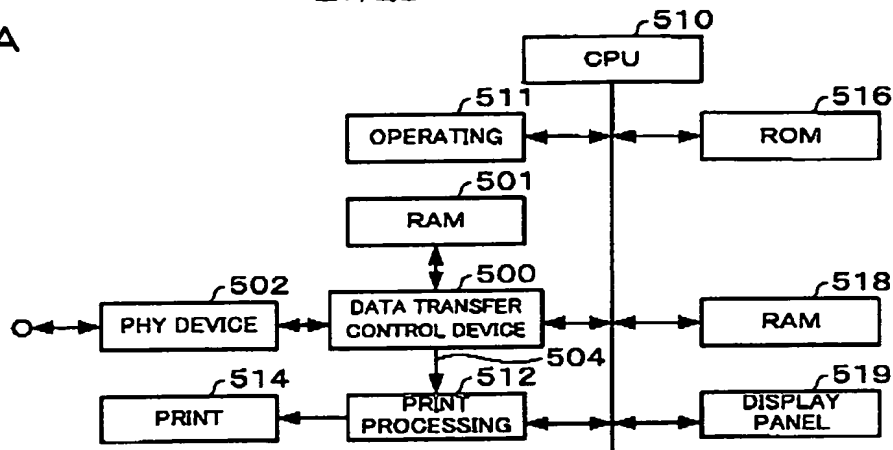


FIG.27B

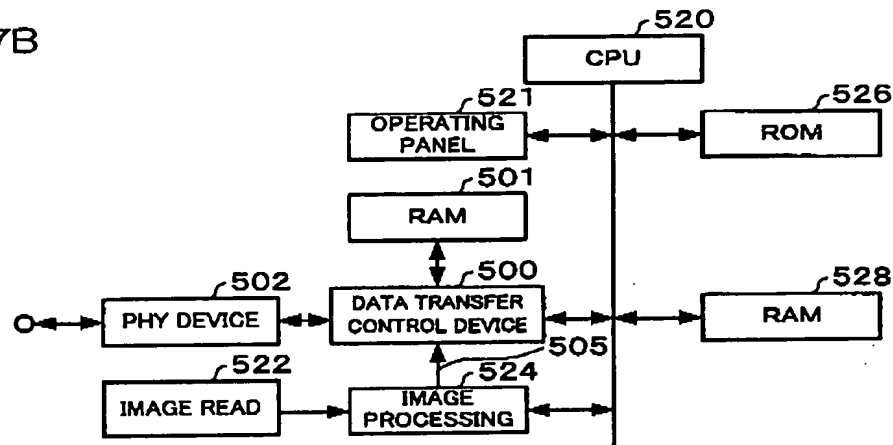


FIG.27C

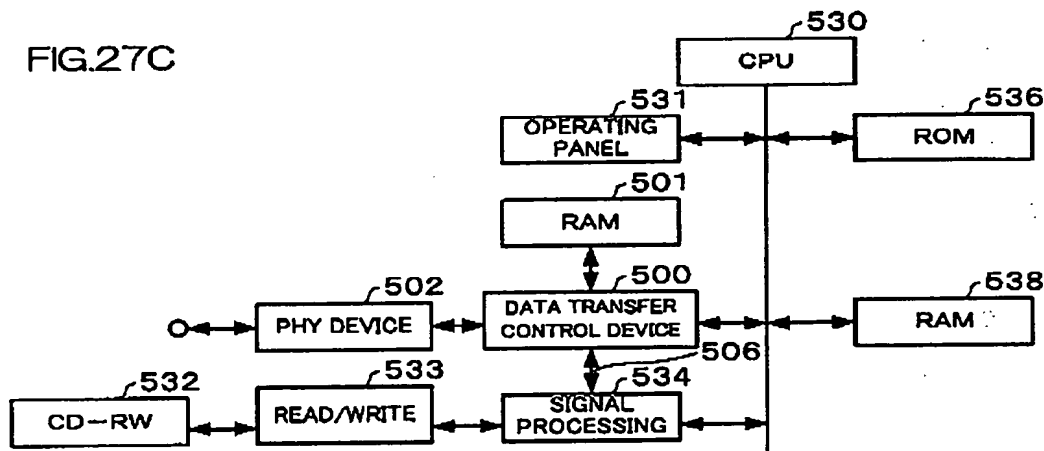


FIG.28A

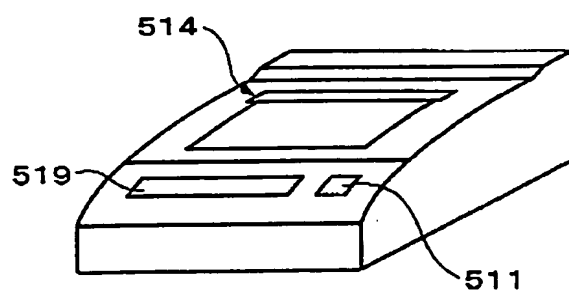


FIG.28B

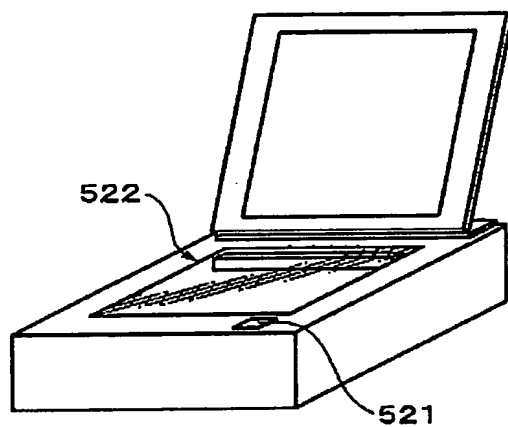


FIG.28C

